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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device with high performance without after-image and blooming.

SOLUTION: This solid-state image pickup device is provided with a photo diode PD and a pixel amplifier 1 provided to each pixel, a horizontal line scanning circuit 2, a vertical line scanning circuit 3, a timing generating circuit 4, a noise canceller circuit 5, a read circuit 6, a boosting circuit 11 that boosts a power supply voltage, and a boosting buffer 12 that drives a gate terminal of a reset transistor(TR) Q1 with a voltage boosted by the boosting circuit 11. Since the TR Q1 is turned on by applying a voltage higher than a usual on-voltage to the gate terminal of the reset TR Q1 at once before the noise canceller circuit 5 detects a reset level, residual charges having been stored in a detection section 25 are discharged to a power supply terminal via a drain terminal of the reset TR Q1, and the effect of the residual charges is not caused in the case of detecting the reset level.

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CLAIMS

[Claim(s)]

[Claim 1] The pixel amplifier which is formed corresponding to each of two or more optoelectric transducers arranged by one train or two or more trains and two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier said timing generating circuit The solid state camera characterized by making said both transfer gates and said reset gates turn on within the same blanking period after the signal according to the charge by which photo electric translation was carried

out by said optoelectric transducer is outputted from said pixel amplifier.

[Claim 2] It is the solid state camera according to claim 1 characterized by having the booster circuit which carries out pressure up of the supply voltage, and making them turn on on an electrical potential difference higher than the usual ON state voltage which generated either [at least] said transfer gate or said reset gate using said booster circuit in case said both timing generating circuits make said transfer gate and said reset gate turn on.

[Claim 3] The pixel amplifier which is formed corresponding to each of two or more optoelectric transducers arranged by one train or two or more trains and two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier It has the booster circuit which carries out pressure up of the supply voltage. Said timing generating circuit The solid state camera characterized by making said reset gate turn on on an electrical potential difference higher than the usual ON state voltage which used and generated said booster circuit within the same blanking period before detecting the output level of said pixel amplifier in a reset condition.

[Claim 4] The pixel amplifier which is formed corresponding to each of two or more optoelectric transducers arranged by one train or two or more trains and two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier It has the booster circuit which carries out pressure up of the supply voltage. Said timing generating circuit The solid state camera characterized by making said

transfer gate turn on on an electrical potential difference higher than the usual ON state voltage generated using said booster circuit in case the output level of said pixel amplifier according to the charge by which photo electric translation was carried out by said optoelectric transducer is detected.

[Claim 5] Said timing generating circuit is a solid state camera according to claim 3 or 4 characterized by making said both transfer gates and said reset gates turn on within the same blanking period after the signal according to the charge by which photo electric translation was carried out by said optoelectric transducer is outputted from said pixel amplifier.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention is aimed at the image sensors which can perform a charge transfer about the solid state image pickup device with which two or more optoelectric transducers were installed successively, without using two or more kinds of electrical potential differences especially.

[0002]

[Description of the Prior Art] There are CCD which switches in order the electrical potential difference impressed to the transfer gate as a typical thing, and transmits stored charge, and CMOS image sensors which transmit stored charge on a single electrical potential difference in a solid state camera.

[0003] CMOS image sensors can be driven by the single power supply of a low battery, there is also little power consumption, and since-izing of the actuation timing circuit can be carried out [on chip], utilization by pocket devices, such as a camera, is expected.

[0004] Drawing 8 is the block diagram showing the outline configuration of the conventional CMOS image sensors. The CMOS image sensors of a graphic display are equipped with the level line scanning circuit 2 which is equipped with Photodiode PD and the pixel amplifier 1 for every pixel, in addition is scanned horizontally, the vertical-lines scanning circuit 3 scanned perpendicularly, the timing generating circuit 4 which controls the timing of these scanning circuits 2 and 3 of operation, the noise canceller circuit 5 which removes the noise component contained in the output of the pixel amplifier 1, a readout circuitry 6, and the load transistor 10.

[0005] The load transistor 10 is arranged for every pixel train, and constitutes source FOROWA amplifier with the pixel amplifier 1 of the selected pixel train.

[0006] Photo electric translation of the light condensed with the non-illustrated optical lens is inputted and carried out to the photodiode PD of drawing 8 , and a charge

(optical generation electron) is generated. This charge can be collected to Photodiode PD during a fixed period, and changes the electrical potential difference of Photodiode PD to it according to the quantity of light. After this voltage signal is amplified with the pixel amplifier 1, it is inputted into the noise canceller circuit 5, and a fixed pattern noise is removed.

[0007] The signal with which the fixed pattern noise was removed is held in the noise canceller circuit 5, reading appearance is carried out to time series by the level line scanning circuit 2, it is amplified with the pixel amplifier 1, and a final pixel signal is acquired.

[0008] The fixed pattern noise mentioned above is a noise made by dispersion in output offset of the pixel amplifier 1, and it generates by dispersion in the threshold electrical potential difference of an MOS transistor.

[0009] The noise canceller circuit 5 offsets a fixed pattern noise by taking the difference of the level of a pixel signal, and the signal level immediately after reset.

[0010] Drawing 9 is the timing chart of the conventional CMOS image sensors of operation, and shows the timing wave of the gate voltage (reset gate electrical potential difference) of a Horizontal Synchronizing signal (H-BLK) and the transistor for reset, the gate voltage (transfer gate voltage) of the transistor for a transfer, a reset hold signal, and a pixel signal hold signal sequentially from the drawing 9 top.

[0011] The reset hold signal and pixel signal hold signal of drawing 9 are a signal used inside the noise canceller circuit 5, within the period when a reset hold signal is high-level, the output level of the pixel amplifier 1 in a reset condition is held, and the output level of the pixel amplifier 1 according to the charge outputted from Photodiode PD is held within the period when a pixel signal hold signal is high-level.

[0012] In both drawing 8 , although the transistor for reset and the transistor for a transfer are omitted, these transistors are connected between Photodiode PD and the pixel amplifier 1. That is, the source terminal of the transistor Q2 for a transfer is connected to the cathode terminal of Photodiode PD, the drain terminal of the transistor Q2 for a transfer is connected to the source terminal of the transistor Q1 for reset, and a power supply terminal Vdd is impressed to the drain terminal of the transistor Q1 for reset. Moreover, both the drain terminal of the transistor Q2 for a transfer and the source terminal of the transistor Q1 for reset are connected to the gate terminal of the transistor Q4 which constitutes the pixel amplifier 1.

[0013] Moreover, the noise canceller circuit 5 compares with the output level of the pixel amplifier 1 when a pixel signal hold signal is high-level the output level of the pixel amplifier 1 when the reset hold signal which shows a wave to drawing 9 is high-level.

[0014] After reset is canceled at the time of day T1 of drawing 9 , the noise canceller circuit 5 holds the signal level at the time of reset between time of day T2 - T3. Next, if it becomes time-of-day T four, the transistor for a transfer will be turned on and the

charge by which photo electric translation was carried out with Photodiode PD will be inputted into the noise canceller circuit 5 through the pixel amplifier 1. Then, the noise canceller circuit 5 holds pixel signal level between time of day T6-T7.

[0015]

[Problem(s) to be Solved by the Invention] When the charge of a large quantity was accumulated in Photodiode PD, the conventional CMOS image sensors could take out no charges outside in the "on" period of the transistor for a transfer, but had the problem that some charges remained in Photodiode PD and an after-image arose. Moreover, when a light intense for Photodiode PD carried out incidence, there was also a problem that the charge by which photo electric translation was carried out caused overflow and a blooming from Photodiode PD.

[0016] Moreover, before the charge picked out from Photodiode PD is inputted into the pixel amplifier 1, it is once accumulated in the detecting element between the gate terminal of the transistor for a transfer, and the gate terminal of the transistor for reset. In order to receive the sensibility of Photodiode PD, a thing with a large capacity of Photodiode PD and a small capacity of a detecting element is desirable, but if it does in this way, an after-image will arise with the charge which it becomes impossible to have taken out all the charges accumulated in Photodiode PD, and remained to Photodiode PD.

[0017] This invention is made in view of such a point, and the object is in offering the solid state camera of high performance without an after-image or a blooming, without complicating the structure of a component.

[0018]

[Means for Solving the Problem] Two or more optoelectric transducers in which this invention was arranged by one train or two or more trains in order to solve the technical problem mentioned above, The pixel amplifier which is formed corresponding to each of two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier said timing generating circuit After the signal according to the charge by which photo electric translation was carried out by said optoelectric transducer is outputted from said pixel amplifier, said both transfer gates and said reset

gates are made to turn on within the same blanking period.

[0019] Moreover, two or more optoelectric transducers in which this invention was arranged by one train or two or more trains, The pixel amplifier which is formed corresponding to each of two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier It has the booster circuit which carries out pressure up of the supply voltage. Said timing generating circuit Said reset gate is made to turn on on an electrical potential difference higher than the usual ON state voltage which used and generated said booster circuit within the same blanking period before detecting the output level of said pixel amplifier in a reset condition.

[0020] Moreover, two or more optoelectric transducers in which this invention was arranged by one train or two or more trains, The pixel amplifier which is formed corresponding to each of two or more of said optoelectric transducers, and amplifies the charge by which photo electric translation was carried out by said corresponding optoelectric transducer, The transfer gate which transmits the charge by which photo electric translation was carried out by said optoelectric transducer to said pixel amplifier, The reset gate which initializes the input voltage of said pixel amplifier on a predetermined electrical potential difference, The timing generating circuit which controls turning on and off of said transfer gate and said reset gate, By detecting difference with the output level of said pixel amplifier according to the charge by which photo electric translation was carried out within the blanking period by the output level and said optoelectric transducer of said pixel amplifier in a reset condition In the solid state camera equipped with the noise canceller circuit which removes the noise component contained in the output of said pixel amplifier It has the booster circuit which carries out pressure up of the supply voltage, and in case said timing generating circuit detects the output level of said pixel amplifier according to the charge by which photo electric translation was carried out by said optoelectric transducer, it makes said transfer gate turn on on an electrical potential difference higher than the usual ON state voltage generated using said booster circuit.

[0021]

[Embodiment of the Invention] Hereafter, the solid state camera concerning this invention is explained concretely, referring to a drawing. Below, CMOS image sensors are explained as an example of a solid state camera.

[0022] (1st operation gestalt) Drawing 1 is the block diagram showing the outline configuration of the 1st operation gestalt of CMOS image sensors. The level line scanning circuit 2 which the CMOS image sensors of drawing 1 are equipped with Photodiode PD and the pixel amplifier 1 for every pixel like the conventional CMOS image sensors shown in drawing 8 , in addition is scanned horizontally, It has the vertical-lines scanning circuit 3 scanned perpendicularly, the timing generating circuit 4 which controls the timing of these scanning circuits 2 and 3 of operation, the noise canceller circuit 5 which removes the noise component contained in the output of the pixel amplifier 1, a readout circuitry 6, and the load transistor 10.

[0023] The load transistor 10 is arranged for every pixel train, and constitutes source FOROWA amplifier with the pixel amplifier 1 of the selected pixel train.

[0024] In the vertical-lines scanning circuit 3, the transistor Q1 for reset, the transistor Q2 for a transfer, the transistor Q3 for selection, and the vertical register circuit 7 are formed. These transistors Q1, Q2, and Q3 are controlled by the signal from the timing generating circuit 4.

[0025] Moreover, in the vertical-lines scanning circuit 3 of this operation gestalt, the pressure-up buffer 12 which drives the gate terminal of the transistor Q1 for reset in the booster circuit 11 which carries out pressure up of the supply voltage, and a booster circuit 11 based on the electrical potential difference by which pressure up was carried out as a configuration which was not in the conventional CMOS image sensors shown in drawing 8 is formed. Turning on and off of the transistor Q1 for reset, the transistor Q2 for a transfer, and the transistor Q3 for selection is controlled by the output of the pressure-up buffer 12.

[0026] The pressure-up buffer 12 outputs the signal depending on the signal depending on the electrical potential difference by which pressure up was carried out in the booster circuit 11, or the usual supply voltage Vdd.

[0027] The source terminal of the transistor Q2 for a transfer is connected to the cathode terminal of Photodiode PD, the drain terminal of the transistor Q2 for a transfer is connected to the source terminal of the transistor Q1 for reset, and supply voltage Vdd is impressed to the drain terminal of the transistor Q1 for reset. Moreover, both the drain terminal of the transistor Q2 for a transfer and the source terminal of the transistor Q1 for reset are connected to the gate terminal of the transistor Q4 which constitutes the pixel amplifier 1. The source terminal of this transistor Q4 is connected to the noise canceller circuit 5, and that drain terminal is connected to the source terminal of the transistor Q3 for selection which drives that gate terminal by the vertical-lines scanning circuit 3.

[0028] Drawing 2 is drawing having shown typically the cross-section structure of the

CMOS image sensors of drawing 1 . Like a graphic display, the n field 21 and the p+ field 22 which constitute Photodiode PD are formed in the interior of a substrate, and the gate field 23 of the transistor Q2 for a transfer is formed in the substrate top face close to this photodiode PD. Moreover, the gate field 24 of the transistor Q1 for reset is formed in the substrate top face close to the gate field 23 of the transistor Q2 for a transfer. The detecting element 25 which consists of a diffusion layer is formed near the substrate front face between the gate field 23 of the transistor Q2 for a transfer, and the gate field 24 of the transistor Q1 for reset. The charge picked out from Photodiode PD is accumulated in this detecting element 25.

[0029] It is the electrogram of the CMOS image sensors in period (1) - (5) which shows drawing 3 in the timing chart of the CMOS image sensors of drawing 1 of operation, and shows drawing 4 to drawing 3 , and actuation of the CMOS image sensors of this operation gestalt is hereafter explained using these drawings. In addition, the axis of ordinate of the electrogram of drawing 4 expresses potential, and it is shown that potential is as high as the lower part of this axis of ordinate.

[0030] After a level shelf-life expires, the timing generating circuit 4 makes the transistor Q1 for reset turn on within the period of (1) of drawing 3 . At this time, the electrical potential difference by which pressure up was carried out in the booster circuit 11 is supplied to the gate terminal of the transistor Q1 for reset. The residual charge accumulated in the detecting element 25 can be discharged outside through the power supply terminal of the transistor Q1 for reset, and residual charge stops existing in a detecting element 25 by supplying a pressure-up electrical potential difference to the gate terminal of the transistor Q1 for reset, as shown in drawing 4 (a).

[0031] Then, within the period of (2) of drawing 3 , the timing generating circuit 4 outputs a reset hold signal, and the noise canceller circuit 5 holds the signal level at the time of reset with this signal. Since the residual charge of a detecting element 25 is removed within the period of (1) of drawing 3 , the signal level at the time of the reset held by the noise canceller circuit 5 stops influencing of residual charge, and dispersion in signal level is controlled. The electrogram within this period becomes like drawing 4 (b).

[0032] Then, the timing generating circuit 4 makes the transistor Q2 for a transfer turn on within the period of (3) of drawing 3 . Thereby, as shown in drawing 4 (c), the charge by which photo electric translation was carried out is accumulated in a detecting element 25 through the transistor Q2 for a transfer with Photodiode PD.

[0033] Then, the timing generating circuit 4 outputs a pixel signal hold signal within the period of (4) of drawing 3 . With this signal, the noise canceller circuit 5 holds the signal level according to the charge by which photo electric translation was carried out with Photodiode PD. The electrogram within this period becomes like drawing 4 (d).

[0034] Then, both the timing generating circuits 4 make the transistor Q1 for reset, and the transistor Q2 for a transfer turn on within the period of (5) of drawing 3 . At this

time, the electrical potential difference by which pressure up was carried out in the booster circuit 11 is supplied to the gate terminal of the transistor Q1 for reset. Thereby, as shown in drawing 4 (e), the residual charge accumulated in Photodiode PD and the detecting element 25 is discharged at a power supply terminal side through each gate terminal of the transistor Q2 for a transfer, and the transistor Q1 for reset.

[0035] Thus, before this operation gestalt detects reset level in the noise canceller circuit 5, since an electrical potential difference higher than the usual ON state voltage is once supplied to the gate terminal of the transistor Q1 for reset and it was made to make this transistor Q1 turn on, the potential of a detecting element 25 becomes high. For this reason, when the transistor Q2 for a transfer is turned on, many charges by which photo electric translation was carried out can be transmitted more to a detecting element 25 from Photodiode PD. Therefore, it can prevent residual charge remaining in Photodiode PD.

[0036] Moreover, although a charge will remain to Photodiode PD as shown in drawing 4 (d) when there are many amounts of incident light Since it was made to make the both sides of the transistor Q2 for a transfer, and the transistor Q1 for reset turn on after making the transistor Q2 for a transfer turn on also in this case and detecting the signal level of a pixel signal, Photodiode PD and the residual charge accumulated in the detecting element 25 can be made to discharge to a power supply terminal side through the drain terminal of the transistor Q1 for reset. Therefore, the high image of the display quality which residual charge stops existing in Photodiode PD, and does not have an after-image is obtained.

[0037] (2nd operation gestalt) The 2nd operation gestalt loses residual charge with the conventional configuration, without forming a booster circuit 11.

[0038] Drawing 5 is the block diagram showing the outline configuration of the 2nd operation gestalt of the CMOS image sensors concerning this invention. In drawing 5 , the same sign is given to the same component as the CMOS image sensors of drawing 1 , and, below, it explains focusing on a point of difference.

[0039] The CMOS image sensors of drawing 5 are constituted almost like the CMOS image sensors shown in drawing 1 except for a point without a booster circuit 11 and the pressure-up buffer 12.

[0040] Drawing 6 is the timing chart of the CMOS image sensors of drawing 5 of operation, and explains actuation of the CMOS image sensors of drawing 5 hereafter using this drawing. With the 1st operation gestalt, although the transistor Q1 for reset was made to once turn on before a reset hold period (period of drawing 3 (2)), this operation gestalt does not have the period which makes the transistor Q1 for reset turn on.

[0041] With the 1st operation gestalt, moreover, after a signal hold period (period of drawing 3 (4)) between synchronizations turns on the transistor Q1 for reset, and the transistor Q2 for a transfer almost simultaneous -- making -- **** (period of drawing 3

(5)) -- this operation gestalt in that the transistor Q1 for reset and the transistor Q2 for a transfer are made to turn on almost simultaneous (period of drawing 6 (4)), although it is the same Also after that, the transistor Q1 for reset holds an ON state.

[0042] Also in this 2nd operation gestalt, in order to make the transistor Q1 for reset, and the transistor Q2 for a transfer both turn on simultaneously after holding a pixel signal, all of Photodiode PD and the residual charge accumulated in the detecting element 25 can be made to discharge outside, and the high image of display quality without an after-image is obtained.

[0043] (3rd operation gestalt) The 3rd operation gestalt is the modification of the 1st operation gestalt, and in case it supplies the charge by which photo electric translation was carried out with Photodiode PD to the pixel amplifier 1, it supplies an electrical potential difference higher than the usual ON state voltage to the gate terminal of the transistor Q2 for a transfer.

[0044] Although the 3rd operation gestalt is the almost same configuration as the CMOS image sensors of the 1st operation gestalt shown in drawing 1 , in case it turns on the transistor Q2 for a transfer, it differs from drawing 1 at the point which supplies the electrical potential difference which carried out pressure up to the gate terminal in the booster circuit 11.

[0045] Drawing 7 is the timing chart of the CMOS image sensors of the 3rd operation gestalt of operation. After the reset hold period (1) of drawing 7 expires, a period (2) is made to turn on the transistor Q2 for a transfer, and the charge by which photo electric translation was carried out with Photodiode PD is led to the pixel amplifier 1 through the transistor Q2 for a transfer. At this time, an electrical potential difference higher than the usual ON state voltage is given to the gate terminal of the transistor Q2 for a transfer. All the charges accumulated in Photodiode PD can be made by this to be able to transmit to the pixel amplifier 1 side, and all the residual charge of Photodiode PD can be discharged.

[0046] (Other operation gestalten) Although drawing 3 showed the example which supplies a pressure-up electrical potential difference a period (1) and (5) to each gate terminal of the transistor Q1 for reset, and the transistor Q2 for a transfer, respectively, at least in one side of these periods, the usual ON state voltage may be supplied to a gate terminal.

[0047] Moreover, with the 1st operation gestalt, although the period (5) of drawing 3 is made to turn on the both sides of the transistor Q1 for reset, and the transistor Q2 for a transfer, this period may be omitted.

[0048] Moreover, although the transistor Q1 for reset and the transistor Q2 for a transfer are made to turn on with the usual ON state voltage, the transistor Q1 for reset and the transistor Q2 for a transfer may be made to turn on in the 2nd operation gestalt on the electrical potential difference which carried out pressure up in the booster circuit 11.

[0049] Moreover, in the 1st operation gestalt, the transistor Q1 for reset may be turned

off during a level shelf-life.

[0050]

[Effect of the Invention] Since it was made to make both the transfer gate and a reset gate turn on according to this invention as explained to the detail above after reading the charge by which photo electric translation was carried out by the optoelectric transducer, all the charges accumulated in the optoelectric transducer can be made to discharge outside, the residual charge of an optoelectric transducer is lost, and the high image of display quality without an after-image is obtained. Even if incidence of the light intense for an optoelectric transducer is carried out or it makes small capacity of the detecting element between the transfer gate and a reset gate for the improvement in sensibility, a blooming and an after-image stop therefore, occurring.

[0051] Moreover, since according to this invention the electrical potential difference higher than the usual ON state voltage was supplied to the transfer gate or a reset gate when making the transfer gate and a reset gate turn on, the residual charge accumulated in the optoelectric transducer or the detecting element can be discharged outside efficiently.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The block diagram showing the outline configuration of the 1st operation gestalt of CMOS image sensors.

[Drawing 2] Drawing having shown typically the cross-section structure of the CMOS image sensors of drawing 1 .

[Drawing 3] The timing chart of the CMOS image sensors of drawing 1 of operation.

[Drawing 4] Electrogram of the CMOS image sensors in period (1) - (5) shown in drawing 3 .

[Drawing 5] The block diagram showing the outline configuration of the 2nd operation gestalt of CMOS image sensors.

[Drawing 6] The timing chart of the CMOS image sensors of drawing 5 of operation.

[Drawing 7] The timing chart of the CMOS image sensors of the 3rd operation gestalt of operation.

[Drawing 8] The block diagram showing the outline configuration of the conventional CMOS image sensors.

[Drawing 9] The timing chart of the conventional CMOS image sensors of operation.

[Description of Notations]

1 Pixel Amplifier

2 Level Line Scanning Circuit

3 Vertical-Lines Scanning Circuit
4 Timing Generating Circuit
5 Noise Canceller Circuit
6 Readout Circuitry
7 Timing Generating Circuit
11 Booster Circuit
12 Pressure-Up Buffer
Q1 Transistor for reset
Q2 Transistor for a transfer
Q3 Transistor for selection
Q4 Transistor for pixel amplifier